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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/976,052	10/15/2001	Hirokatsu Hayashi	HITA.0110	1675

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EXAMINER	
NGUYEN, MINH T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,052	HAYASHI ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *20-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicants' response to the restriction requirement has been received and entered in the case. The election with traverse is acknowledged. The Applicant's argue that claims 1-19 are directed to the species which are not patentably distinct is also acknowledged. The following is a detailed Office Action of claims 1-19.

Drawings

2. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because:

(i) it exceeds 150 words,

(ii) it compares the invention with the prior art, i.e., first sentence.

Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because of the following informalities: page 18, lines 13-16 refers Fig. 1 as a first preferred embodiment and lines 21-23 refers Fig. 4 as a first preferred embodiment. Appropriate correction is required.

6. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification does not have proper antecedent basis the first circuit, second circuit recited in claim 1, the delay means recited in claim 2, the "circuit" and "MOS transistor", "the number of stages" recited in claim 3, the "high resistance element" recited in claim 5, the first and second inverters recited in claims 7, the third inverter recited in claim 8, the delay means recited in claim 9.

Claim Objections

7. Claims 16-17 are objected to under 37 CFR 1.75(c) as being in improper form because a multiple dependent claim. See MPEP § 608.01(n). Accordingly, the claims 16-17 are not been further treated on the merits.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the term "second signal" recited on line 8 lacks clear antecedent basis, i.e., it is unclear if this is referring to the second signal recited on line 5. The word "whose" recited on line 14 is unclear, i.e., it is unclear if it is used to refer to the source-drain routes of which transistors. The phrase "said n-channel type MOS transistor" lacks antecedent basis, i.e., it is unclear which n-channel type MOS transistor it is referring to. The phrase "supplying said fourth signal from said third output terminal" recited on the last line is misdescriptive, i.e., the third output terminal is not supplying the fourth signal but rather the third output terminal receives the fourth signal from the second circuit.

As per claim 2, due to the antecedent basis problem noted herein above, the recitation cannot be understood. It is unclear how the delay means can control those recited transistors which are the first and second p-channel MOS transistors and the first and second n-channel MOS transistors. It appears that the Applicants try to combine several embodiments into one claim by using the words "and", "or" which are so difficult to determine the metes and bounds of the claim without doubt, therefore, the claim is seen as being indefinite. The response should provide a concise explanation of which elements constitute the delay means and how these

elements can satisfy the recited function which is to control the first and second p-channel MOS transistors and the first and second n-channel MOS transistors.

As per claim 3, the claimed subject matters recite in the claim cannot be understood, i.e., it is unclear where the recited "circuit", the recited "MOS transistor", the "number of circuit stages" come from. The response should point out which elements shown in Fig. 1 corresponding to these recited elements.

As per claim 7, the phrase following the term "being comprised" recited on line 5 cannot be understood, i.e., it is not clear which one, the inverter or the first circuit, being comprised those elements. It appears that it is referring to the inverter 11 shown in Fig. 1, however, the inverter 11 shown in Fig. 1 does not have more than two transistors (the claim recites four transistors).

As per claim 9, the recited third inverter appears misdescriptive because as shown in Fig. 1, the circuit has only two inverters which are 11 and 13.

As per claim 10, the claim is indefinite because of the lack of proper antecedent basis noted in section 6 above. It is further unclear if the recited "delay means" is the same as the "delay means" recited in claim 2. In the response, please indicate which elements shown in Fig. 1 refers to the delay means recited in claim 2 and which elements shown in Fig. 1 refers to the delay means recited in claim 10.

As per claim 12, the recited "logical threshold" on line 19 lacks antecedent basis. i.e., it is unclear which element(s) the recited "logical threshold" is referring to. Claim 12 also further has the problems discussed in claim 1 above.

As per claim 18, this claim is rejected as being incomplete since the claim does not have a structural relationship between the first and second level conversion circuits, i.e., it is merely a "catalogue of elements" which is not permissible. *See In re Collier, 158 USPQ 266.*

As per claims 13-19, these claims have various problems discussed in claims 1-3, 7 and 9-10.

The rest of the claims are further rejected because of the indefiniteness of independent claims discussed herein above.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,300,835, issued to Assar et al.

As per claim 1, Assar discloses a level conversion circuit (Fig. 2) comprising:

a first circuit (transistors 272, 273, 274, 275) including a first input terminal (gate of 274) for receiving a first signal OEN* having a first signal amplitude, a first output terminal (drain of 275) for supplying a second signal (on line 223) having a second signal amplitude greater than said first signal amplitude (because the first circuit is a level shifter) and being in the same phase as said first signal (the structure of the level shifter satisfies this limitation), and a second output terminal (drain of 274) for supplying a third signal (on line 222) having a second signal

amplitude greater than said first signal amplitude and being in the phase reverse to said first signal; and

a second circuit (transistors 252-255, 256-259, 250 and 251) including a first p-channel type MOS transistor (256), a second p-channel type MOS transistor (257), a first n-channel type MOS transistor (258) and a second n-channel type MOS transistor (259) whose source-drain routes are connected in series between a first voltage terminal (NVDD) and a second voltage terminal (GND), and the drain of said first p-channel type MOS transistor (257) and the drain of said n-channel type MOS transistor (258) are connected to a third output terminal (PAD, through the buffer comprises transistor 250 and 251),

wherein said second circuit forms a fourth signal (at line 201) having said second signal amplitude on the basis of the signal variation of said second signal supplied from said first output terminal of said first circuit or of said third signal supplied from said second output terminal of said first circuit, whichever is faster in signal level change, and supplying said fourth signal from said third output terminal (PAD).

As per claim 2, in sofar as understood, Assar further discloses a delay means (transistors 260-263) for delaying said second signal supplied from said first output terminal of said first circuit or said third signal supplied from said second output terminal of said first circuit to control said second p-channel type MOS transistor and said first n-channel type MOS transistor, or said first p-channel type MOS transistor and said second n-channel type MOS transistor.

As per claim 3, in sofar as understood, the recited "circuit" reads on transistors 250 and 251 and the recited "MOS transistor" reads on transistor 251.

As per claims 4, since the gates of the recited transistors are connected to the second or the third signals, the state of said second p-channel type MOS transistor or first n-channel type MOS transistor in said second circuit varies with change in said second signal or third signal supplied from said first circuit.

As per claim 5, a high resistance element (transistor 253) for pull-up use and a high resistance element (259) for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.

As per claim 6, the recited limitation is described in column 6, lines 25-30, i.e., using SPICE program to design the sizes and widths of transistors.

As per claim 7, the recited first inverter reads on transistors 276 and 277, the recited second inverter reads on transistors 264 and 265.

As per claim 8, the recited limitation is met since it is merely the operation of the level shifter circuit having the structure recited in claim 7.

As per claim 9, the recited third inverter reads on transistors 270 and 271.

As per claim 10, in sofar as understood, the recited delay means reads on transistors 260-263.

As per claim 11, the recited limitation is met since it is merely the operation of the circuit.

As per claims 12-13, these claims are rejected for the same reasons noted in claim 1.

As per claims 14-15, these claims are rejected for the same reasons noted in claims 1, 1, respectively.

As per claims 16-17, these claims are improper dependent claims. It appears that the recited limitations are merely intended use of the level shifter circuit when the level shifter is operated, and therefore, no patentable weight is given.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,300,835, issued to Assar et al.

As per claim 18, Assar discloses a level shifter as discussed in claim 1 herein above, but he does not explicitly disclose a further second level shifter (another species).

However, combining two level shifters in an integrated circuit is seen as an obvious modification for generating of other species as admitted by the Applicants (see paper number 7, election of species).

As per claim 19, the recited limitation is merely an intended use of the circuit.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Nos. 6,149,319, 5,723,986, 6,351,173 disclose various level shifter circuits.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
April 5, 2003